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Analysis and Simulation of Power Stage Voltage Controller Model Using Feedback Compensator

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ABSTRACT (10 PT)

This paper presents the design of power stage voltage control model under digital feedback compensator. The power high performance electronic system has to maintain stable voltage supply even though rapid change in power consumption in the load terminals. Hence, the efficient transfer function parameters selection of digital control system in the power stage converter is the most important in practices. To provide effective suppression in the output voltage corresponding to fast load change, correct feedback circuit with powerful transfer function has been suggested in this work. Close to output tracking of reference sinusoidal voltage is achieved by proposed techniques with fast rejection to sudden load variation. Furthermore, the obtained control system is robust against to reservations in the input DC voltage. The model is tested and evaluated under different performance in both transient operation and steady state requirements.

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1. INTRODUCTION

Nowadays, power electronics and control systems are a core program in the demand of many engineering researchers due to high important of these types of studies [1]. Digital signal controllers and applications to system control and processing is presented to achieved improved the effect of load change on the input supply [2]. In exists time, beside the improvement and developing the theoretical part, the performance of controller is verified via digital simulation and implementation of operation amplifiers systems [3]. The applications of power electronics was presented since long time ago by mean of construction, assembly, program development and prototype experimental testing [4]. As the controller applications are based on structures, the mathematical part was used to guide the digital controller design under technical literature and prototype development [5]. In many types of electronic device supply system, the buck converter is widely used due to its small size, low weight and high power efficiency [6]. The most important parameters in this type of converter is the ability to keep constant voltage level on the output terminal with variation load current [7, 8, 9, 10]. Many techniques were used to stabilize the output voltage level such as current mode, voltage mode and converter controller techniques [11, 12, 13, and 14]. The transfer function modeling has presented for digital controller of converter using analog prototype with alternative procedures of transfer function selection [15, 16, 17]. Texas instruments board select a transfer function of digital control device with the following blocks parameters [18, 19, 20, 21]:

a. Voltage divider
b. Propagation delay of control algorithms
c. Converter power stages
d. Anti aliasing filters

The power stage converter equivalent circuit showing in Figure 1 use small signal model to describe buck converter with regard to influence of output conductance variations on output level [22, 23, 24]. This model was used to simplify the design of transfer function of the control block without output impedance [25].

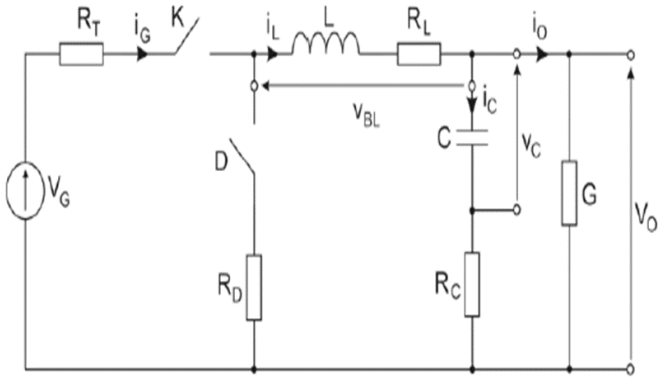

Figure 1: power stage equivalent circuit [25]

Other important coefficients in the converter transfer function are the resonant frequency of small signal model which is used to determine the position of poles in the frequency domain of transfer function [26, 27, 28].

2. METHOD

Figure 2 shows the digital control of power stage voltage model designed by MATLAB/SIMULINK environments. This model illustrates the tuning of high performance digital controller under close bandwidth to the frequency of sampling process. The SIMULINK block set has been used to design and run the voltage control for electronic devices.

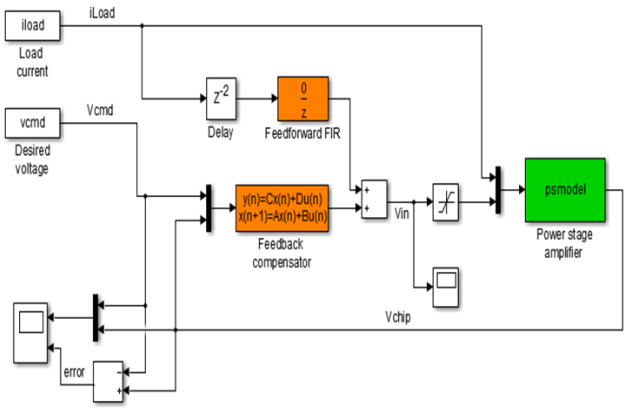

Figure 2: Power Stage Voltage controller model

The amplifier of power stage is designed as a second order linear system with frequency response showing Figure 3 and Figure 4 with and without controller respectively. The voltage Vchip that delivered to the device used to track the set point Vcm which is insensitive to load current change Iload. The structure of controller contains an efficient feedback and disorder feed forward compensators. The input voltage of the amplifier (Vin) is imitate to Vmax= 12V and the sampling rate of the controller equal to 1e-7 seconds (10 MHz). Clearly, the effect of digital controller in stabilization of input voltage with high drop in the load current is highlight in the system performance.

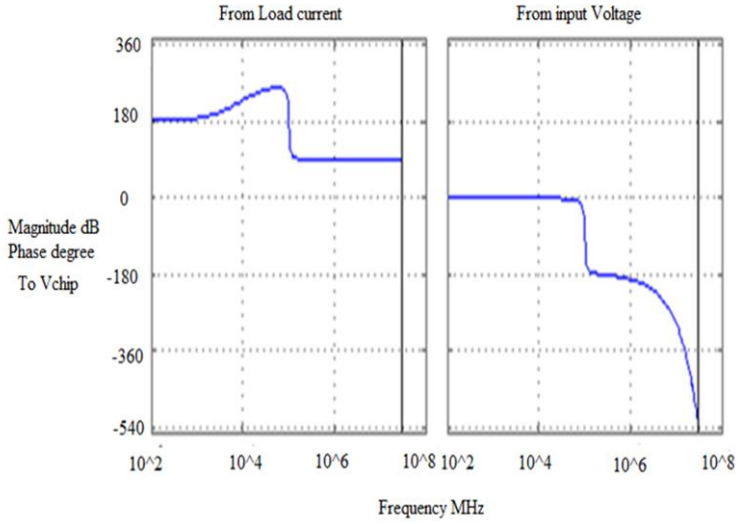

Figure 3: Power stage amplifier Frequency response without controller

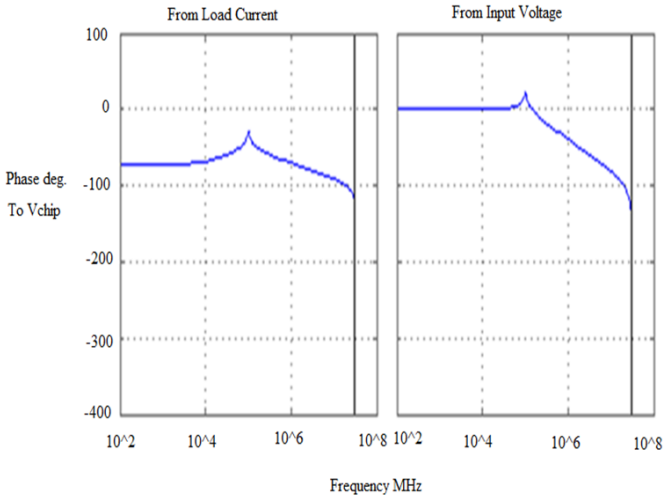

Figure 4: Power stage amplifier Frequency response with existing controller

The challenging of this model is due to controller bandwidth that should be within Nyquist frequency of about 30MHz. Hence, to overcome the aliasing phenomena due to discrete time of continuous time controller, it's important to tune the controller straightly in discrete time form. The response of power stage should exist in the desired set point voltage Vcm with nearly five sample duration. Figure 5 shows the peak error of about 50% in tracking requirements to provide the controller goals.

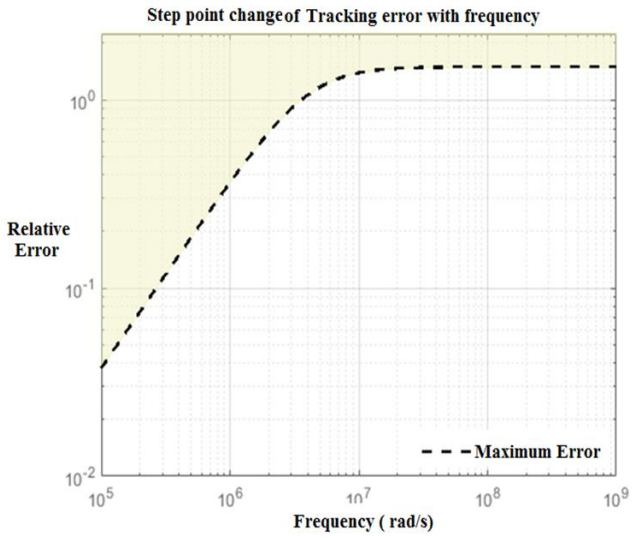

Figure 5: peak error in step point change of tracking technique

The rejecting of load disturbance current should be fast requested by power stage under gain requirements from load current (Iload) to chip voltage (Vchip). For efficient disturbance rejection, the gain should be very low at low frequency and high control effort could be provided by high performance. In case of ramp mode, Vcm specified from zero to one in 250 sample duration to overcome the drumming of saturation limitations. The rate limiting filter has been used to design the ramp which required gain less than input rate limiting.
Seven dB gain and 45 degree phase at the input has been tuned to ensure the robustness of the model. At the end, the feedback compensator has a propensity to terminate the resonance by notch away. This deposit inversion could lead to weak results in case of resonance frequency is not accurately recognized or subjected to the deviations. Hence, minimum closed loop damping of about 0.5 is used to aggressively moist the resonance mode.

3. RESULTS AND DISCUSSION

To tune the parameters of designed controller, the system tuner (systune) has been used with the respect to the model requirements. The s1Tuner interface has been used to configure the simulink model and specify two tunable blocks for the model sample time (Tm) linearization. The feed forward compensators are implemented by using first order finite impulse response (FIR) filter which is automatically parameterizes the feedback compensators as third order state space mode. The constraints of margin and damping requirements have been maintain to meet the remaining conditions. The hard constraints less than one has been considered to satisfy the model conditions which are nearly satisfy all constraints close to 1. The verification of these constrains graphically has been done for every parameters as illustrated in Figure 6.

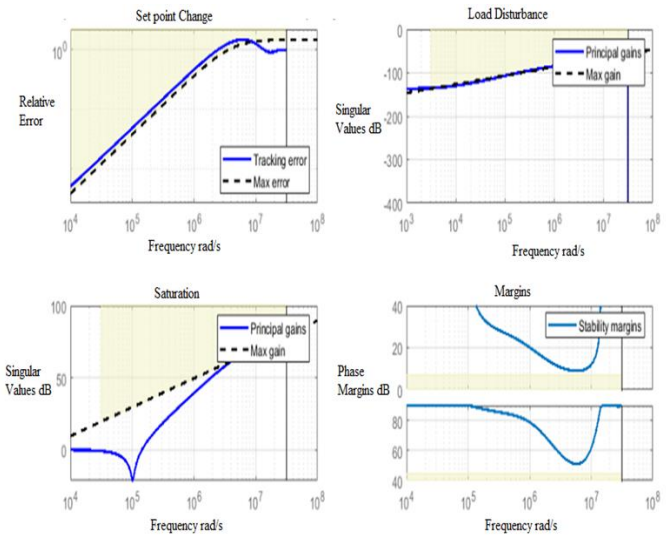

Figure 6: parameters verifications

The validation of the design in liner domain is performed by use s1Tuner interface command to plot the close loop response between Vcm and iLoad disturbance current as shown in Figure 7 and Figure 8.

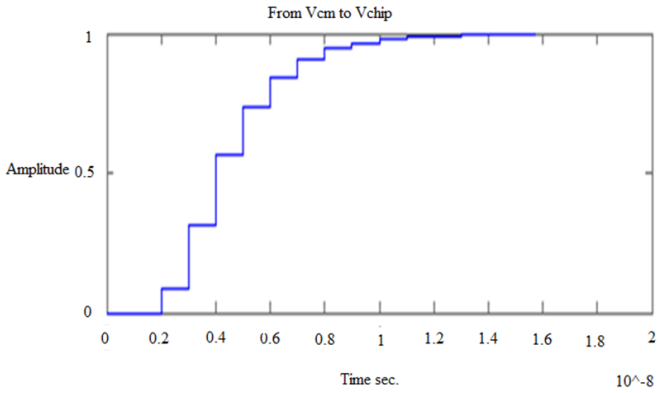

Figure 7: voltage response to step command from Vcm and Vchip

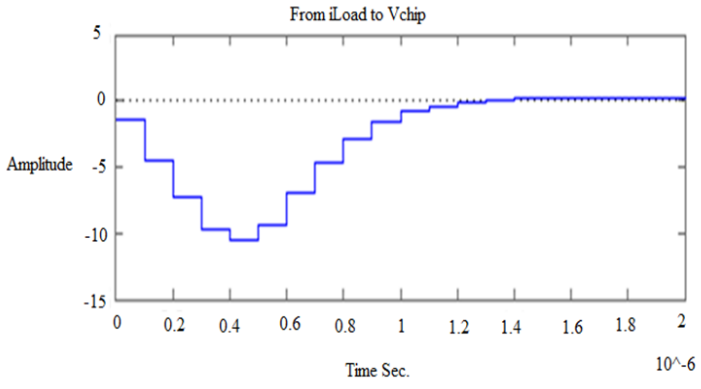

Figure 8: rejection of step disturbance in load current from iLoad to Vchip

To compute the open loop response at the input part and apply to the feedback compensator responses, the get loop transfer has been used as show in Figure 9 and Figure 1 for magnitude and phase response respectively.

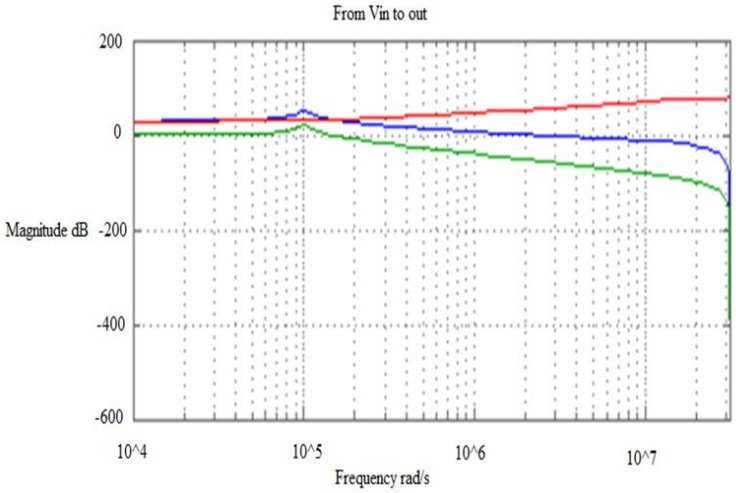

Figure 9: Magnitude response of open loop response, input and Compensator

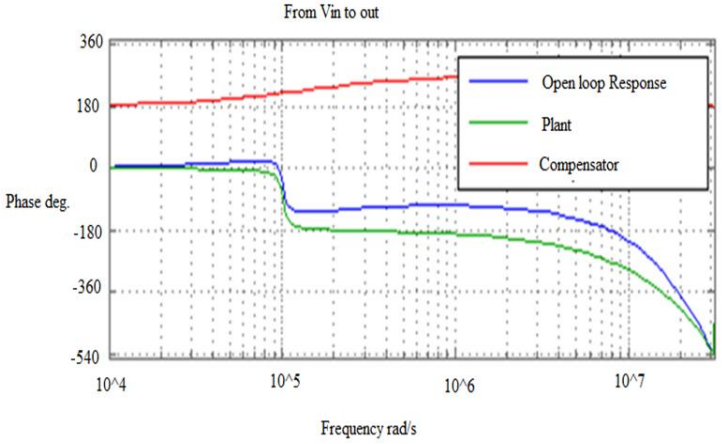

Figure 10: Phase response of open loop response input and compensator

The desired bandwidth and speed of responses has achieved by applying the tuned parameters values to the simulink model. The non linear simulation results illustrated in Figure 11 shows that the control signal Vin maintain within saturation bound for set point tracking. The Amplitude of input voltage Vin throughout set point tracking phase is illustrated in Figure 12.

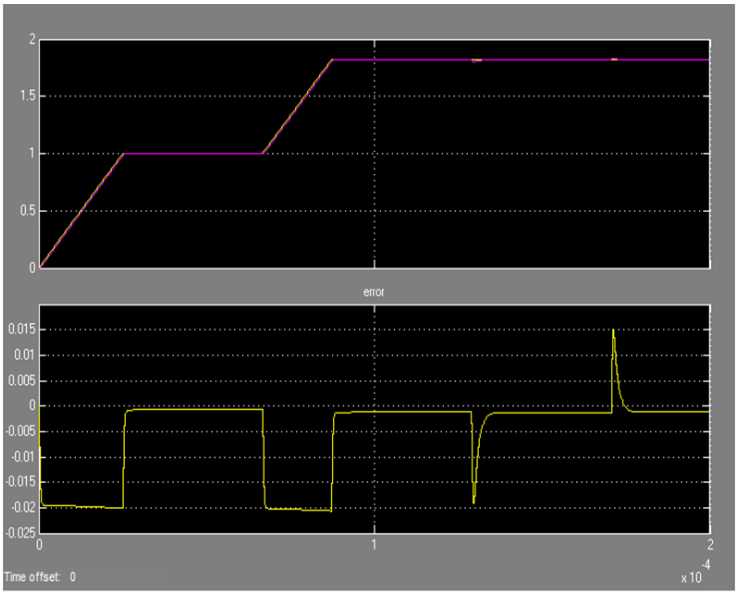

Figure 11: Ramp command response and step load disorder.

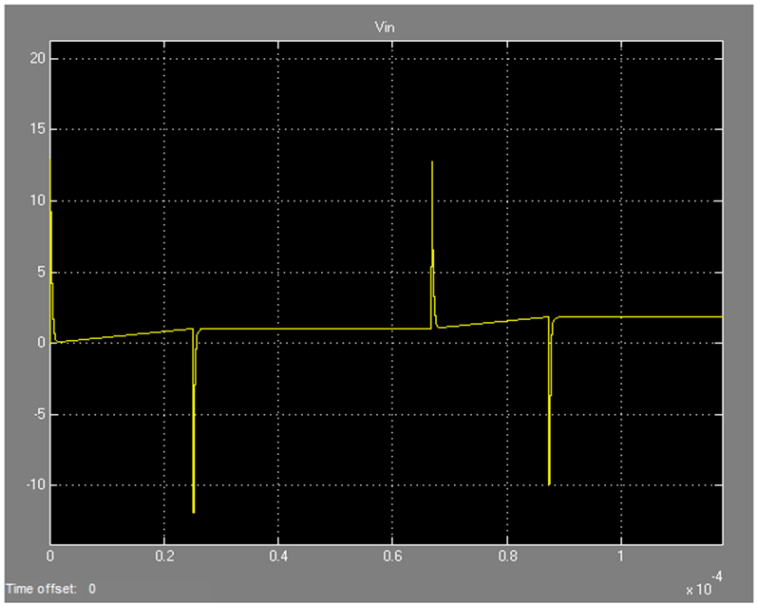

Figure 12: Amplitude of input voltage Vin during set point tracking phase.

4. CONCLUSION

This paper introduced the design and simulation of digital power stage voltage controller model using feedback compensator to improve and develop the effect of load current variation on the input supply. The possibility of influence changing in load current reduction is confirmed by feedback techniques without any aliasing phenomena. The suggested design of digital control system for power inverter is capable to operate in existence of fast variation in the load current and input voltage. This structure was tested and evaluated by mean of a feedback compensator ability to produce a sinusoidal at 30MHz which is expose high quality of output signal to react a high speed nonlinear variation of load with response time. The model has established to be strong against large variation in input direct current voltage. Hence, the digital signal processing could be used to compute the complex of control algorithms.

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